REMARKS

The Office Action of November 5, 2002 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested.

Claims 1-24 are pending, claims 1, 4, 11, 14 and 21 having been amended, and claims 23-24 having been added.

Claims 1-22 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 5,059,815 to Bill et al. Applicant submits that the amended claims obviate the rejection.

Claims 1-22 recite a voltage generating/transferring circuit comprising a first capacitor having one end which is connected to an output node, and another end which receives a first oscillation signal. Applicant submits that Bill is completely devoid of teaching or suggesting a voltage generating/transferring circuit having such a feature. For example, in Figure 1A of Bill, capacitor CL is connected to ground (0 volts) and the oscillation signal is not input thereto.

At least for the reason discussed above, Applicant submits that the claims are patentable over Bill and respectfully requests that the rejection to claims 1-22 be withdrawn.

New claims 23-24 depend from claims 1 and 11, respectively, and are patentable for at least the reasons discussed above.

All rejections having been addressed, Applicant submits that the application is now in condition for allowance, and a notice to that effect is earnestly solicited.

Applicant hereby petitions for any other fees required to maintain the pendency of this ase, except for the Issue Fee, and such fee is to be charged to Deposit Account No. 19-0733,

If for any reason the Examiner is unable to allow the application on the next Office Action and feels that an interview would be helpful to resolve any remaining issues, the

Examiner is respectfully requested to contact the undersigned attorney for the purpose of arranging such an interview.

Respectfully submitted,

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MARKED-UP VERSION SHOWING THE AMENDMENTS

IN THE CLAIMS:

The claims were amended as follows:

1. (Twice Amended) A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first voltage; and

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal,

wherein each boost unit has input and output portions, a second transistor having a gate and a drain connected to the input portion and a source connected to the output portion, and a second capacitor in each boost unit connected to the input portion, and a gate of said first transistor is connected to the input portion of one of the boost units.

4. (Amended) A voltage generating/transferring circuit according to claim 1, wherein a ~~first~~ second oscillation signal is input to an even-numbered boost unit from the input node, a ~~second~~ third oscillation signal is input to an odd-numbered boost unit from the input node, and the ~~first~~ second and the ~~second~~ third oscillation signals have opposite phases or different timings.

11. (Amended) A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first voltage; and

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal,

wherein each of the boost units has input and output portions, a second transistor having a gate and a drain connected to the input portion and a source connected to the output portion, and a second capacitor in each of the boost units connected to the input portion, a charge moves between the output portion of one of the boost units and the input portion of another of the boost units, and a gate of said first transistor is connected to the input portion of one of the boost units.

14. (Amended) A voltage generating/transferring circuit according to claim 11, wherein a ~~first~~ second oscillation signal is input to an even-numbered boost unit from the input node, a ~~second~~ third oscillation signal is input to an odd-numbered boost unit from the input node, and the ~~first~~ second and the ~~second~~ third oscillation signals have opposite phases or different timings.

21. (Amended) A voltage generating/transferring circuit comprising:

a boost unit group including at least a first boost unit and a second boost unit series-connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first voltage; and

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal,

wherein each of said first and second boost units has an input portion, an output portion, a second transistor having both a gate and drain connected to the input portion and a source connected to the output portion, and a second capacitor in each of said first and second boost units connected to the input portion, the source of the second transistor of said first boost unit being directly connected to the input portion of said second boost unit, and a gate of said first transistor being connected to the input portion of one of said first and second boost units.

Claims 23 and 24 have been added.